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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/389,826	09/03/1999	HANS U. SCHROEDER	PHN-17.073	5932

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EXAMINER
NADAV, ORI

ART UNIT	PAPER NUMBER
2811	

DATE MAILED: 10/01/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/389,826	SCHROEDER ET AL.	
	Examiner	Art Unit	
	ori nadav	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12 June 2002* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-9* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-9* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Specification

1. The disclosure is objected to because of the following informalities: on page 5, line 15, reference number 18 is the gate electrode and should not be designated as "n type well 18".

Appropriate correction is required.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

3. Claims 1-9 are rejected under 35 U.S.C. 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. The specification recites a gated diode. There is no support for at least two gated diodes, as recited in claims 1 and 7-8.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which the subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 1-9, insofar as in compliance with 35 U.S.C. 112, are rejected under 35 U.S.C. 103(a) as being unpatentable over Ker et al. (5,572,394).

Ker et al. teach in figure 9 a semiconductor device having an ESD protection means being an SCR and a gated electrode, provided in a surface area (P-SUBSTRATE) of a first conductivity type having a single well (N-WELL) of a second conductivity type, wherein a surface zone (P+) of the first conductivity type is forms a first anode and cathode area of the SCR element, the surface area has a surface zone (N+) of the second conductivity type, noted as a first zone, situated remotely from the well and forming a second anode and cathode area of the SCR element, the gated diode containing a gate insulated from the surface area and a highly doped (N+) second conductivity type surface zone aligned to the gate, noted as a second zone, which aligned surface zone partly overlaps the well of the second conductivity type, wherein the second zone stretches out only along a part of the periphery of the well, whereas the first zone is provided along at least another part of this periphery which is free from the second zone.

Regarding the claimed limitation of a single well, although figure 9 of Ker et al. depicts three wells, figure 9 also depicts a single well. The claimed limitations do not include protection means consisting of a single well. Therefore, the broad recitation of the claim does not preclude the protection means from comprising more than a single well. Ker et al. do not teach two gated diodes. It would have been obvious to a person of ordinary skill in the art at the time the invention was made to use two gated diodes in Ker et al.'s device in order to use the device in an application which requires plurality of protection circuits.

Regarding claim 2, Ker et al. teach in figure 11 the gate of the gated electrode substantially stretches out only along the part of the periphery of the well along which also the second zone stretches out.

Regarding claim 3, the gated diode having a further surface zone (N+) of the second conductivity type deposited in the surface area of the first conductivity type and forming the other of the source/drain zones of the transistor, wherein the first zone being situated at a shorter lateral distance from the surface zone provided n the well than the further surface zone.

Regarding claim 4, although Ker et al. do not explicitly disclose a further zone and a first zone form a second conductivity type zone this feature is inherent in Ker et al.'s device, because Ker et al.'s structure is identical to the claimed structure.

Regarding claim 5, the first and second conductivity types are p and n conductivity types, respectively, wherein the first zone and the first conductivity type zone in the well form the cathode and anode of the SCR element, respectively.

Regarding claim 6, Ker et al. teach the well of the second conductivity type is arranged in the form of a longitudinal zone, the surface zone of the first conductivity type is formed by a longitudinal zone in the well of second conductivity type which well has in its center an opening at the position of which a highly doped zone of the second conductivity type is provided which forms a contact area for the well of second conductivity type.

Regarding claims 7 and 8, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to form the at least two gated diodes on the right-hand end of the longitudinal zone which comprises the insulated gate and the highly doped second conductivity type surface one which partly overlaps the well of the second conductivity type, wherein the at least two gated diodes are arranged as a MOS

transistor having a further zone of the second conductivity type in Ker et al.'s device, since the location of the two gated diodes is a matter of design choice within the skills of an artisan, subject to routine experimentation and optimization.

Regarding claim 9, Ker et al. teach the cathode of the SCR is provided along the part of the periphery of the well of the second conductivity type that is free from the at least two gates.

Response to Arguments

6. Applicant argues on page 4 that reference numbers 17 and 18 of figure 6 provide support for the claimed limitation at least two gated diodes, as recited in claims 1 and 7-8.

Figure 6 is a cross section along line VI--VI in figure 4, wherein one gate electrode 18 is formed in a half circle shape. Reference numbers 17 and 18 of figure 6 are n+ diffusion region and a gate electrode, respectively, and not two gate electrodes, as argued by applicant. Therefore, there is no support for at least two gated diodes, as recited in claims 1 and 7-8.

7. Applicant argues on pages 5 and 6 that there is no motivation to use two gated diodes in Ker et al.'s device and such modification is not within the knowledge available to an artisan.

It is well known in the semiconductor industry that a protection device does not include one transistor, but plurality (usually thousands) of transistors. Therefore, it is well within the skills of an artisan to include two transistors (gated diodes) in Ker et al.'s device. Furthermore, applicant did not explicitly disclose in the specification the uniqueness and the importance of using two gated diodes. Therefore, it is held that such modification can be within the skills of an artisan.

Conclusion

8. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL.** See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the

shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Papers related to this application may be submitted to Technology center (TC) 2800 by facsimile transmission. Papers should be faxed to TC 2800 via the TC 2800 Fax center located in Crystal Plaza 4, room 4-C23. The faxing of such papers must conform with the notice published in the Official Gazette, 1096 OG 30 (November 15, 1989). The Group 2811 Fax Center number is (703) 308-7722 and 308-7724. The Group 2811 Fax Center is to be used only for papers related to Group 2811 applications.

Any inquiry concerning this communication or any earlier communication from the Examiner should be directed to *Examiner Nadav* whose telephone number is **(703) 308-8138**. The Examiner is in the Office generally between the hours of 7 AM to 4 PM (Eastern Standard Time) Monday through Friday.

Any inquiry of a general nature or relating to the status of this application should be directed to the **Technology Center Receptionists** whose telephone number is **308-0956**

TOM THOMAS
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800

Ori Nadav

September 26, 2002